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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,583	06/20/2001	Carol Lemlein	1527-US	3971
7590	03/26/2004		EXAMINER	
Legal Department Teradyne, Inc. 321 Harrison Avenue Boston, MA 02118			LAMARRE, GUY J	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,583	LEMLEIN ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 January 2004.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-18 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on 12 January 2004 is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____.

2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) Other:

DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicants' amendment of 12 Jan. 2004. [The petition for 1-month extension of time, concurrently filed, is granted.]

1.1 Claims 7, 10 are amended; Claims 11 is added Claims 1-11 remain pending.
1.2 The prior art rejections of record are maintained in response to Applicants' amendment of 12 Jan. 2004.

1.3 The rejections under 35 U.S.C. 112 of record are withdrawn in response to Applicants' amendment of 12 Jan. 2004.

1.4 The objections of record are withdrawn in response to Applicants' amendment of 12 Jan. 2004.

Response to Arguments

2. Applicants' arguments of 12 Jan. 2004 have been fully considered and are not persuasive because **Conner (USP # 5,794,175)** teaches parallel test means that reduces the number of pins in e.g. Figs. 2-3. By sharing common stimulus application pins, implying common timing circuitry means, deskew circuitry is shared by more than one channel in a parallel test mode. System is optimized in parallel test mode and is less than optimal in non-parallel test mode.

Claim Rejections - 35 USC ' 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3.0 This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly

owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

3.1 Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (hereinafter admitted prior art) in view of Lopez (US 45,111,208), Catiller (US 4,429,389) and Conner (US 5,794,175).

Referring to **Claims 1, 3, 7, 9-11**, an admitted prior art discloses "a channel module 22", (page 1, line 22) including "a channels 28" (page 2, line 3), and "a programmable delay circuitry comprising a deskeew circuit 30, performing the identical functions" (page 2, line 4). The admitted prior art does not explicitly teach and point out to provide a plurality of channels, but does not suggest or mention to limit the quantity of channels by single channel. Lopez discloses the plural-channel system and teaches to provide a plurality of channels ("plural-channel signal carrying system" 1see column 2, lines 56, 57)). Catiller teaches to provide a channel parallelism for testing Integrated Circuit (IC) memories having row and column drivers. "A parallel array of exclusive OR gates" (a plurality of exclusive OR gates /e.g. see column 12, lines 64, 65) are arranged so that the "output line of each OR gate" provides one address information bit to a bus which simultaneously carries parallel bits of address information. Conner discloses a plurality of "channel modules 46", including "a plurality of outputs" (see Fig. 3) and "data lines", and "a programmable delay circuit". Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the admitted prior art with the teaching of Lopez (US 45,111,208) and of Catiller (US 4,429,389) by using the plurality of channels, because one of ordinary skill in the art would simply use plurality principles for identically intended channels including a deskeew circuit shared by more than one of the channels, performing the appropriate identical functions in order to minimize apparatus hardware architecture (configuration) and costs.

Claim 2 depends from respective claim 1, hence inherit the rejection in claim 1. Also, according to claim 2, it is well known and would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a channel module by an integrated circuit formed with more than one channel, because one of ordinary skill in the art would simply use well known integration principles applicable to the integrated circuit (IC) industry.

According to claim 3, Lopez discloses a calibration of plural-channel system teaches to determine the level of accuracy and to correct the inaccuracy (e.g., col. 12, lines 19, 20). Lopez does not explicitly teach and point out to provide operations with the deskew data, but Conner describes that "circuitry making calibration and deskew adjustments are generally incorporated into the tester to ensure that the test signals are actually generated at the programmed times".

The admitted prior art provides steps of the deskew data collection and storage , and referring to the step of optimization, Lopez teaches that "in any of the foregoing plural channel systems, optimum operation of the system is obtained when the design characteristics of the respective channels are maintained. A calibration process and equipment are utilized to provide optimum operation".

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the admitted prior art with the teaching of Lopez (US 45,111,208) and of Catiller (US 4,429,389) and Conner (US 5,794,175) to operate with the deskew data, because one of ordinary skill in the art would simply use the deskew data format for collecting, optimizing and storing such data, considering common principles applied to the calibration and test equipment and apparatus in compliance with the calibrating and testing device functional operability.

Claims 4-6 depend from respective claim 3, hence inherit the rejection in claim 3. Also, referring to claims 4-6, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to provide the averaging the deskew data and/or utilizing the individual deskew data, because one of ordinary skill in the art would simply use the averaging principles inherent for optimization processes (e.g. in compliance with the theory of optimality by Bellman), as well as, utilization of the individual data applicable to the optimization principles.

Referring to claims 7-11, claims 7-11 are similar to claims 1-6, and are rejected based on the same rationale thereof.

Conclusion

4. THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Guy J. Lamarre, P.E.
Patent Examiner
3/22/04
